REMARKS

The Office Action dated December 18, 2003, has been received and reviewed.

Claims 1-34 are currently pending in the above-referenced application. Of these, claims 4, 9, and 23-34 have been withdrawn from consideration as being directed to a non-elected invention. Claims 1-3, 5-8, and 10-22, which remain under consideration, currently stand rejected.

Claims 10 and 11 have been canceled without prejudice or disclaimer.

Reconsideration of the above-referenced application is respectfully requested.

Information Disclosure Statement

Please note that an Information Disclosure Statement was filed in the above-referenced application on November 21, 2003, but that the undersigned attorney has not yet received any indication that the references cited in the Information Disclosure Statement have been considered in the above-referenced application. It is respectfully requested that the references cited in the Information Disclosure Statement of November 21, 2003, be considered and made of record in the above-referenced application and that an initialed copy of the Form PTO/SB/08A that accompanied that Information Disclosure Statement be returned to the undersigned attorney as evidence of such consideration.

Objections to the Drawings Under 37 C.F.R. § 1.84(p)(4)

The drawings have been objected to for failing to comply with the requirements of 37 C.F.R. § 1.84(p)(4). Specifically, it has been asserted that each of Figs. 1, 1A, 6B, 6C, 8A, 8D, 9A, 10A, and 10B includes multiple reference characters that designate the same element. It has also been asserted that reference characters 18 and 118 have "been used to designate multiple different parts." Office Action of December 18, 2003, page 2.

It is respectfully submitted that each of Figs. 1, 1A, 6B, 6C, 8A, 8D, 9A, 10A, and 10B complies with the requirements of 37 C.F.R. § 1.84(p)(4). In particular, it is respectfully submitted that each of reference characters 10, 110, 210, 210', 310, and 410 designates a chip-scale package, while reference characters 18, 118, 218, 218, 318, and 418 each designate a

carrier substrate, which are merely parts of the illustrated chip-scale packages, and reference character 126 designates a substantially planar layer, which is merely a part of the carrier substrate 118 shown in Figs. 1A, 6B, and 6C.

Further, it is respectfully submitted that neither reference character 18 nor reference character 118 has been used to designate anything other than a carrier substrate.

For these reasons, it is respectfully submitted that multiple reference characters have not been used to designate the same elements and that none of the reference characters has been used to designate multiple, different elements. It is, therefore, respectfully submitted that the drawings comply with the requirements of 37 C.F.R. § 1.84(p)(4).

Accordingly withdrawal of the 37 C.F.R. § 1.84(p)(4) objections to the drawings is respectfully requested.

Objections to the Drawings Under 37 C.F.R. § 1.83(a)

The drawings have also been objected to for assertedly failing to comply with the requirements of 37 C.F.R. § 1.83(a). In particular, the drawings have been objected to for failing to show "the elected species wherein said introducing comprises chemical vapor depositing, and wherein said defining is effected before said positioning . . ."

It is respectfully submitted that Fig. 3 illustrates "defining effected before . . . positioning" and that Figs. 4 and 4A depict embodiments where chemical vapor depositing may be used to introduce conductive material into contact with bond pads or other contacts pads of a semiconductor device.

Accordingly, it is respectfully submitted that drawings are in compliance with the requirements of 37 C.F.R. § 1.83(a) and, thus, requested that the 37 C.F.R. § 1.83(a) objection to the drawings be withdrawn.

Objections to the Drawings Under 37 C.F.R. § 1.84(p)(5)

Figs. 6B and 6C of the drawings have also been objected to under 37 C.F.R. § 1.84(p)(5) for failing to show reference character 118.

Appropriate corrections have been made to these drawings by including reference character 118 and an appropriate lead line in each of Figs. 6B and 6C.

Therefore, withdrawal of the 37 C.F.R. § 1.84(p)(5) objections to Figs. 6B and 6C is respectfully requested.

Rejections Under 35 U.S.C. § 112, First Paragraph

Claim 10 has been rejected under 35 U.S.C. § 112, first paragraph, for allegedly failing to comply with the enablement requirement.

Claim 10 has been canceled without prejudice or disclaimer, rendering the rejection thereof moot.

It is, therefore, respectfully requested that the 35 U.S.C. § 112, first paragraph, rejection of claim 10 be withdrawn.

Rejections Under 35 U.S.C. § 102(e)

Claims 1-3, 5-8, and 10-20 stand rejected under 35 U.S.C. § 102(e).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Hashimoto

Claims 1-3, 5-8, and 11-20 have been rejected under 35 U.S.C. § 102(e) for reciting subject matter which is purportedly anticipated by the disclosure of U.S. Patent 6,255,737 to Hashimoto (hereinafter "Hashimoto").

The description of Hashimoto is directed to, among other, things, a process that includes applying a preformed sheet of polyimide 64 to a wafer 60 carrying a plurality of semiconductor devices. FIGs. 13A and 13B; col. 11, lines 45-48. Apertures 64a are formed through the preformed sheet 64 following application thereof to the wafer 60 to expose bond pads 62 of the

semiconductor devices through the preformed polyimide layer 64. FIG. 13C; col. 11, lines 49-52. Conductive material 68 may then be introduced into the apertures 64a and into contact with the bond pads 62. FIG. 13D; col. 11, lines 49-54.

Independent claim 1, as amended and presented herein, recites a method for fabricating a chip-scale package. The method of independent claim 1 includes positioning a preformed polymeric film over a semiconductor device. The preformed polymeric film includes at least one aperture that extends substantially longitudinally therethrough. When the preformed polymeric film is positioned over the at least one semiconductor device, the at least one aperture is in substantial alignment with a corresponding bond pad of the semiconductor device. The method of amended independent claim 1 also includes introducing conductive material into the at least one aperture.

In contrast to amended independent claim 1, Hashimoto lacks any express or inherent description of positioning a preformed polymeric film that includes at least one aperture therethrough over a semiconductor device. Hashimoto also includes no express or inherent description of positioning the polymeric film so that at least one aperture therethrough is in substantial alignment with a corresponding bond pad of the semiconductor device.

Since Hashimoto does not expressly or inherently describe each and every element of amended independent claim 1, Hashimoto cannot anticipate each and every element of amended independent claim 1, as would be required to maintain the 35 U.S.C. § 102(e) rejection of amended independent claim 1. It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(e), amended independent claim 1 recites subject matter which is allowable over the subject matter described in Hashimoto.

Claim 11 has been canceled without prejudice or disclaimer, rendering moot the rejection thereof.

Each of claims 2, 3, 5-8, and 12-20 is allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Claim 5 is additionally allowable since Hashimoto neither expressly nor inherently describes defining an aperture through a preformed polymeric film before positioning the same over a semiconductor device.

Claim 19 is further allowable since Hashimoto does not expressly or inherently describe placing a preformed polymeric film on at least a portion of a peripheral edge of a semiconductor device.

Claim 20 is additionally allowable since Hashimoto lacks any express or inherent description of placing polymeric material at least laterally adjacent a conductive structure. Instead, the description of Hashimoto is limited to forming "outermost layer[s] (protective layer[s])," which partially surround conductive structures. Col. 12, lines 50-52 and 62-64.

Gilleo

Claims 1, 10, and 19 stand rejected under 35 U.S.C. § 102(e) for being directed to subject matter which is purportedly anticipated by the subject matter described in U.S. Patent 5,971,253 to Gilleo (hereinafter "Gilleo").

The description of Gilleo is directed to apparatus for testing semiconductor devices and to methods for assembling such apparatus with semiconductor devices and test equipment.

In one embodiment, a connection component 20 of Gilleo, depicted in FIG. 1 thereof, includes a dielectric sheet 22 with holes 24 formed therethrough. Col. 4, lines 28-56. A conductive shell 30 is disposed within each hole 24. Col. 4, line 57, to col. 5, line 57. Each conductive shell 30 is coated with an electrically conductive bonding material 38. Col. 5, lines 58-63. The shells 30 and conductive bonding material 38 are introduced into the holes of the dielectric sheet 22 before the dielectric sheet 22 is positioned over a semiconductor device. Col. 6, lines 18-31.

In another embodiment, shown in FIG. 5 of Gilleo, a connection component 220 includes a dielectric sheet 222 with holes 224 formed therethrough and shells 230 extending through each hole 224. Col. 9, lines 38-42. Each shell 230 is a hollow structure with an open end that is configured to face a bond pad of a semiconductor device and a closed end that is positioned to face away from the semiconductor device. Col. 9, lines 45-51. Each shell 230 is introduced into a hole 224 and filled with a mass 228 of soft, electrically conductive material prior to assembly of the connection component 220 with a semiconductor device. *See id.*, col. 10, lines 1-4.

Amended independent claim 1 recites, among other things, that conductive material is introduced into at least one aperture of a preformed polymeric film before the preformed polymeric film is positioned over a semiconductor device.

As the conductive shells that are described in Gilleo must be introduced into the holes of a dielectric sheet before the sheet is positioned over a semiconductor device, Gilleo does not and cannot expressly or inherently describe, or anticipate, the requirement of amended independent claim 1 that such introduction occur after the preformed polymeric film is positioned.

Accordingly, under 35 U.S.C. § 102(e), amended independent claim 1 recites subject matter which is allowable over that described in Gilleo.

Claim 10 has been canceled without prejudice or disclaimer, rendering the rejection thereof moot.

Claim 19 is allowable, among other reasons, for depending directly from claim 1, which is allowable. Claim 19 is also allowable because Gilleo does not expressly or inherently describe that a dielectric sheet thereof may be placed on at least a portion of a peripheral edge of a semiconductor device.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1-3, 5-8, and 10-20 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

Claims 21 and 22 stand rejected under 35 U.S.C. § 103(a) for being drawn to subject matter which is purportedly unpatentable over the teachings of Hashimoto, in view of teachings from U.S. Patent 6,294,407 to Jacobs (hereinafter "Jacobs").

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference

> (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Claims 21 and 22 are both allowable, among other reasons, for depending indirectly from claim 1, which is allowable.

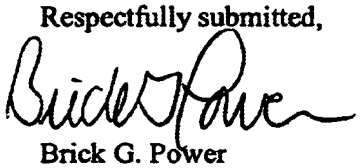
ELECTION OF SPECIES REQUIREMENT

It is respectfully submitted that independent claim 1 remains generic to all of the species of invention of the second group that was identified in the Election of Species Requirement in the above-referenced application. In view of the allowability of these claims, claims 4 and 23-34, which have been withdrawn from consideration, should also be considered and allowed. M.P.E.P. § 806.04(d).

CONCLUSION

It is respectfully submitted that each of claims 1-8 and 12-34 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



Brick G. Power
Registration No. 38,581
Attorney for Applicants
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: March 18, 2004

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